ULTRAHIGH-SPEED RESONANT-TUNNELING
ANALOG-TO-DIGITAL CONVERTER
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ABSTRACT
A flash analog-to-digital converter, consisting of resonant-tunneling ternary quantizers and ternary-to-binary encoder circuits, is proposed. SPICE simulation exhibits a possible 10-GHz operation with reduced device counts and power dissipation, which are due to its compact circuit configuration.

1. INTRODUCTION
Analog-to-digital converters (ADCs) with multi-GHz sampling frequencies have been required for ultrahigh-speed instrumentation. Recently, they are also expected to play a crucial role in wireless communication systems, particularly in realizing future software-defined radio with digital IF/RF architecture [1]. There have been several attempts to fabricate ultrahigh-speed ADCs by using SiGe or InP heterojunction bipolar transistors [2] [3]. As an alternative approach, we have proposed the use of InP-based resonant-tunneling diodes (RTDs) [4] [5], which are known as the fastest semiconductor device among others [6].

In this paper, we propose an ADC that employs RTD-based complex gates. To convert a three-level thermometer code into a binary Gray code, we develop a new scheme consisting of ternary-signal subtraction. This is achieved by combining the MML (monostable-multistable transition logic) quantizer [7] with another RTD-based circuit, MOBILE (monostable-bistable transition logic element) [8]. This MML/MOBILE complex gate is proved to be suitable to build an ultrahigh-speed flash ADC with low power dissipation.

2. BASIC IDEA
An intrinsic performance limitation in flash ADCs is related to the number of comparators that increases exponentially (2^n-1) as the bit resolution n increases. To solve this problem, we previously proposed to introduce a multi-level intermediate signal between the analog input and binary output, which makes a flash ADC quite compact [4]. Figure 1 shows such an ADC with ternary quantizers followed by a ternary-to-binary encoder. MSB stands for the most significant bit, while LSB is the least significant bit.

Figure 2 shows the encoding scheme we have proposed in this paper. We subtract one three-level signal from the other to obtain, for example, the “0-1-0-1-0” MSB-2 output.
3. 4-bit ADC WITH MML/MOBILE COMPLEX GATE

Now a 4-bit ADC will be presented. Figure 3 shows an MML ternary quantizer and its transfer characteristics. To vary threshold voltages, we attached an HFET with the controlling voltage $V_c$ in parallel to the input HFET with the analog input $x_n$. Two threshold voltages, $V_1$ and $V_2$, decreases as $V_c$ increases, because of the linear summation of the two HFET drain currents.

For the second least-significant-bit (LSB+1), we used an MML/MOBILE complex gate shown in Fig. 4. The buffers are used as level shifters. $V_{c,c}$ is smaller than $V_{c,d}$ so that the two threshold voltages in “c” are larger than corresponding ones in “d”. This results in the output waveform as explained in Fig. 2.

For the LSB, we used another MML/MOBILE complex gate as shown in Fig. 5. Four controlling voltages were designed such that $V_{c,g} < V_{c,h} < V_{c,e} < V_{c,f}$. To obtain the output waveforms needed for the ADC operation, these voltages also satisfied the following conditions: $V_{c,g} < V_{c,c} < V_{c,h}$, and $V_{c,e} < V_{c,d} < V_{c,f}$.

4. SIMULATION RESULTS AND DISCUSSION

Now SPICE simulation results will be presented for a 4-bit flash ADC using the MML/MOBILE complex gates described above. We assumed InP-based 0.15-µm HFET and RTD technology [4]. The peak current density of RTDs was $2 \times 10^5$ A/cm$^2$ and the peak-to-valley current ratio was 10. The HFET unity-current-gain cutoff frequency $f_T$ and the maximum oscillation frequency $f_{MAX}$ were 120 GHz and 200 GHz, respectively.

In the present circuit, both MML quantizers and MOBILE circuits needed clocked supply voltages. In this simulation, the clock $\phi_1$ for the quantizer increases with the rise time of 100 ps, as shown in Fig. 6(a). The quantizer output started increasing immediately after $\phi_1$ rose, and evolved into three levels depending on the analog input value, as depicted in Fig. 6(b). After $\phi_1$ settled, the clock $\phi_2$ for the MOBILE started increasing with the same rise time. The simulation result shows that the MOBILE outputs evolved into two levels as $\phi_2$ reached the stable state. It should be noted that we used $\phi_1$ and $\phi_2$ as two-phase clocks in the pipelined architecture. Our recent study also shows that the ADC operates even if the rise time decreases to 50 ps. These results indicate that this ADC can operate at sampling frequencies as high as 10 GHz.
Figure 7 shows simulated outputs of a present 4-bit ADC. Plotted values for each bit were sampled at 20 ps after the clock $\phi_2$ stopped rising. Note that 4-bit operation is clearly confirmed.

Table 1 compares 4-bit ADC performance. Since the MML/MOBILE complex gate made the encoder circuit quite compact compared with the previous one, the device count was much reduced. The decrease in power dissipation is due to the reduction in the number of SCFL current path from 28 to 13, as well as drain current optimization.

Table 1 Comparison of 4-bit ADCs

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed (GHz)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Present*</td>
<td>~120</td>
<td>10</td>
</tr>
<tr>
<td>Previous [4]*</td>
<td>~240</td>
<td>10</td>
</tr>
<tr>
<td>SiGe [2]</td>
<td>&gt;1000</td>
<td>8</td>
</tr>
</tbody>
</table>

* Simulation results

Figure 6. MML quantizer and $M^2$-MOBILE complex gate (simulation).

Figure 7. 4-bit outputs of a present ADC (simulation).
5. CONCLUSION

We proposed a flash analog-to-digital converter that consisted of resonant-tunneling ternary quantizers and ternary-to-binary encoder circuits. SPICE simulation exhibited a possible 10-GHz operation with reduced device counts and power dissipation, which are due to its compact circuit configuration.

REFERENCES